
Shortie VHDL for Synthesis

Emerging applications ranging from AI for IoT, embedded vision, hardware security, 5G communications, and industrial/automotive automation are redefining hardware requirements for developers designing products that operate at the network Edge.

To support these applications, Edge devices need hardware options that offer:

- Low power consumption
- High performance
- High reliability
- Small form factor

The design of digital circuits in this scale needs a powerful hardware description language which offers different levels of abstraction, so an engineer can create a digital hardware design in a quick and effective way. VHDL fulfils these requirements.

VHDL is a strongly typed hardware description language which prohibits typical programming mistakes in the coding phase. Usually, VHDL is used on the register transfer level (RTL) to design digital circuits of any complexity. Apart from the language constructs for synthesis, VHDL offers a wide range of functionality to describe complex verification models. Thus, it is possible verify digital designs from simple gate up to complex System-on-Chip (SoC) before going to lab tests.

This shortie provides an overview of synthesis relevant aspects of the VHDL hardware description language based on the IEEE Std. 1076-2008 language revision, including introduction Language Concept, Design Flow and Modelling Techniques. The theoretical knowledge will be deepened with demonstrations and examples presented by the trainer.

Course Objectives:

- Introduction to the general FPGA Architecture
 - Introduction to Lattice Radiant Design Flow
 - Learn an all parallel computer language to describe digital circuits
 - Learn VHDL-2008 language constructs mainly for synthesis
 - Understand parallel execution model
 - Understand how VHDL translates to gates and circuits
 - Create digital circuit descriptions for FPGAs
 - Run the synthesis and implementation tool flow in Lattice Radiant / Diamond Software
 - Divide a design into hierarchical units
 - Demonstrations and Examples
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Agenda

Introduction to the general FPGA Architecture

Introduction to Lattice Radiant Design Flow

Designing FPGAs

- Traditional Methods
- HDL based Method
- The VHDL Design Flow

VHDL Concept

- Language Concept
- Structural Description
- Behavior Description
- The VHDL Type Concept
- VHDL for Synthesis
- VHDL for Verification

Designing with VHDL

- Design Units
- Entity & Architecture
- Package
- Hierarchy and Components
- Operators

Modeling Behaviour

- Process
- Sequential Statements
- Concurrent Statements

Preview VHDL for Verification

Example

- Various Examples given during the presentation

Applicable Technologies

- Lattice Semiconductor CrossLink NX Series FPGAs

Software / Hardware used

- Lattice Semiconductor Radiant Design Software,
- Lattice Semiconductor CrossLink-NX Evaluation Board

Prerequisites

- Basic Knowledge in digital circuit design is welcome.

Workshop Format and Duration

- Shortie, 4 hours

Participant Documents provided

- Presentation Work-Book
- Exercise Lab-Book

