Shortie Radiant Design Flow

Emerging applications ranging from AI for IoT, embedded vision, hardware security, 5G communications, and industrial/automotive automation are redefining hardware requirements for developers designing products that operate at the network Edge.

To support these applications, Edge devices need hardware options that offer:

• Low power consumption

• High performance

• High reliability

• Small form factor

CrossLink™-NX family of low-power FPGAs can be used in a wide range of applications, and are optimized for bridging and processing needs in Embedded Vision applications – supporting a variety of high bandwidth sensor and display interfaces, video processing and machine learning inferencing. It is built on Lattice Nexus FPGA platform, using low-power 28 nm FD-SOI technology. It combines the flexibility of an FPGA with the low power and high reliability (due to extremely low SER) of FD-SOI technology.

Course Objectives:
The Lattice Radiant® software is a complete toolset for designing for Lattice Semiconductor's FPGAs. This Shortie leads you through all the basic steps of designing, constraining, implementing, and debugging designs targeted to the Lattice CrossLink-NX™ (LIFCL) device family.
This Shortie demonstrates how to:

- Create a new Radiant software project.
- Customize IP using IP Catalog.
- Verify functionality with simulation.
- Set timing and location constraints.
- Process the design.
- Analyse power consumption.
- Analyse static timing.
- Create on-chip debug logic.

Agenda

Introduction

General Radiant Design Flow Overview

Detailed Radiant Design Flow Overview

Create a new Radiant Project

Add HDL Code

Verify Functionality with Simulation

Set the Timing Constraints

Set Location Assignments

Process the Design

Examine the Layout

Analyse Power Consumption

Add On-Chip Debugger Module

Example Design and Evaluation Board used

Let's do the Example

Labs

- The theoretical content is supplemented by exercises presented by the trainer and carried out by the participant.

Applicable Technologies

- Lattice Semiconductor CrossLink NX Series FPGAs

Software / Hardware used

- Lattice Semiconductor Radiant Design Software,
- Lattice Semiconductor CrossLink-NX Evaluation Board

Prerequisites

- Basic Knowledge in digital circuit design is welcome.

Workshop Format and Duration

- Shortie, 4 hours

Participant Documents provided

- Presentation Work-Book
- Exercise Lab-Book
